



Jitter Performance of XRT91L31
OC12 / 3 SONET / SDH Transceiver

AN-91L31-03-01

Version 0.2

Network & Transmission Products



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1. Objective:

XRT91L31 performance evaluation

2. References:

XRT91L31 Datasheet

3. Summary:

The jitter performance of EXAR XRT 91L31 is measured for Jitter Tolerance, Intrinsic Jitter Generation and Jitter Transfer.

The EXAR 91L31 with standard optics has excellent Jitter Generation, and Jitter Tolerance performance with plenty of margin and in the low bandwidth mode, passes Jitter Transfer specification.

4. Equipment used:

4.1. Hardware:

Agilent OmniBer (AN104) 718, 725

E3610A DC Power Supply

XRT91L31 evaluation boards, Computer, Xtals, SFPs:

XRT91L31USB.exe, T91L31_Rev1P00.hex

5. Discussion:

5.1. Setup description:

5.2. Setup description:

Figure 1 shows the basic connection of the setup. Please see the Evaluation board manual for the description of the board and the details of the test procedures.

The optically received data (via the SFP) are fed to the RXIN data pins of the XRT91L31 and the outputs TXDO pins are connected to optical signal via the SFP, and connected to the input of the Omniber SONET /SDH tester. The Agilent Omniber 718 or 725 performs all the Jitter tests (Jitter Generation, Jitter Transfer and Tolerance tests.) Various standards SFPs can be used e.g. OCP, Infineon (Finisar), as well as other vendors.

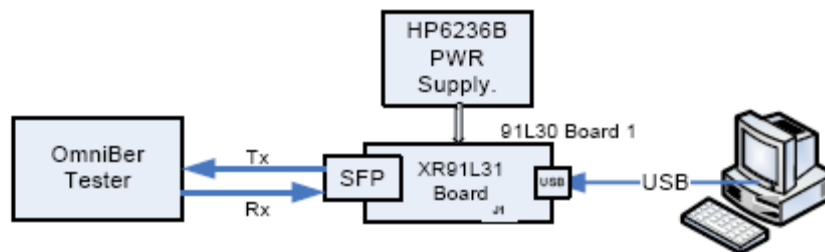


Figure 1 Setup Block Diagram

Figure 1 Omniber settings (Jitter)

5.3. Test Equipment settings:

5.3.1. Jitter Tolerance



Figure 2 OmniBer settings (Jitter)

5.3.2. Jitter Transfer (Jitter Tabs):



Figure 3 OmniBer settings (Jitter)

5.3.3. Jitter Transfer (Main Tabs)



Figure 4 Omniber settings Main Tab for OC3

5.3.4. Jitter Generation Filter settings OC12



Figure 5 Jitter generation for OC12

5.3.5. Jitter Generation Filter settings for OC3



Figure 6 Jitter Generation settings for OC3

5.4. Evaluation Board GUI settings for different measurements:

5.4.1. Jitter Generation (OC3 example)

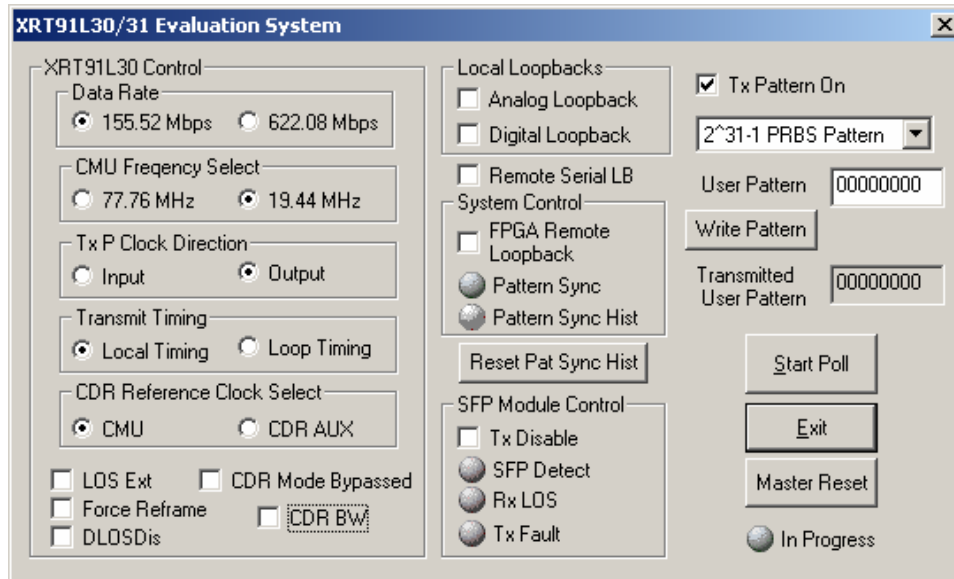


Figure 7 GUI settings for Jitter Generation for OC3

In this case, Jitter Generation results are being measured on random data stream (a PRBS pattern 2^{31}) generated by the FPGA on the evaluation board and fed through the transmit section of the XRT91L31. The same setup is used for the VSC8117 device.

5.4.2. GUI Settings for Jitter Transfer/Tolerance:

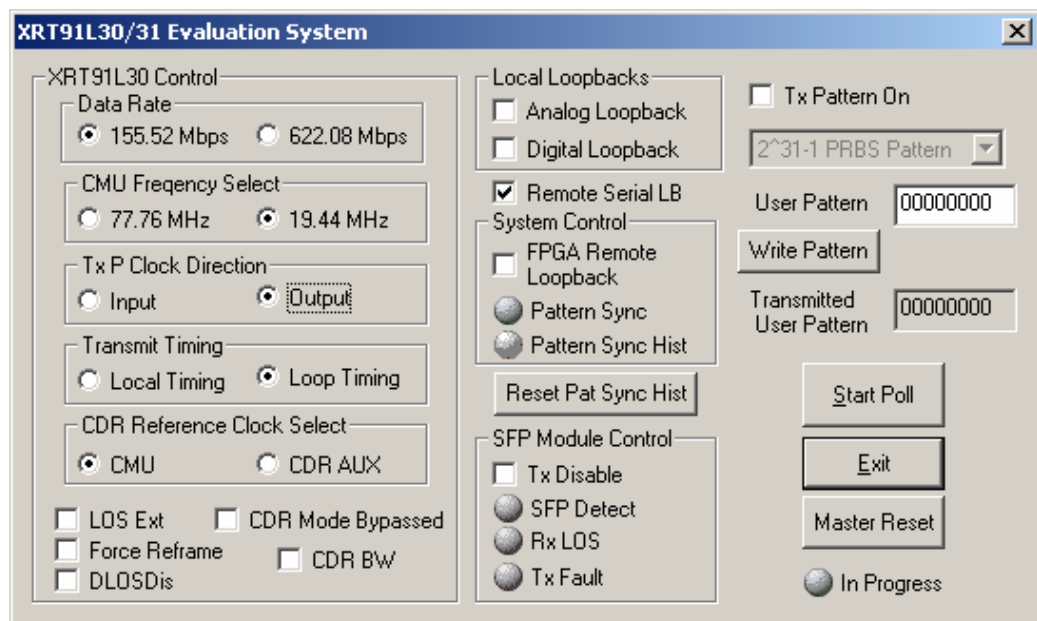


Figure 8 GUI settings for Jitter Tolerance or Jitter Transfer Measurement



In this setup, the device under test is configured to be in remote line loopback mode. In this mode, the recovered clock and data from the receiving path are looped back to the transmit path (internal recovered loop timing). In this case the tester performs the jitter tests with its own data pattern and the jitter modulation that it injects to measure the output performance of the device.

In the case of Jitter Transfer test, as a normal procedure, the tester has to be self calibrated (connecting its output to its input) prior to taking the results from the device under test.

The XRT91L31 has selectable bandwidth. In high bandwidth mode, Pin 15 is HIGH (compatible with the Vitesse VSC 8117), the jitter transfer is marginal. Note that the VSC8117 fails the jitter transfers specification miserably.

When configured to be in low bandwidth mode (Pin 15 is Low), the XRT91L31 meets the Jitter Transfer specification also. Jitter Tolerance and Jitter Generation remain comparably good. See results in next section.

6. Results:

6.1. XRT91L31 Jitter Tolerance Results

6.1.1. OC12 Jitter Tolerance Results:

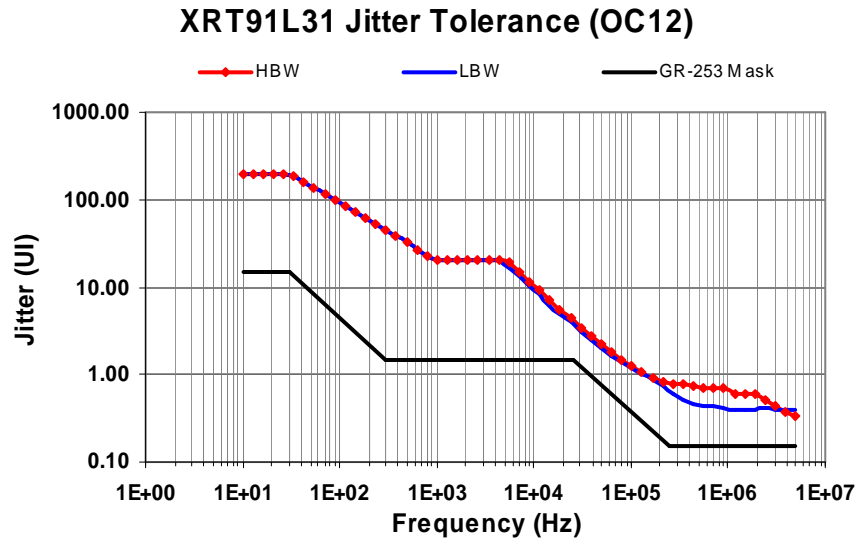


Figure 9 Jitter tolerance for OC12

6.1.2. OC3 Jitter Tolerance Results:

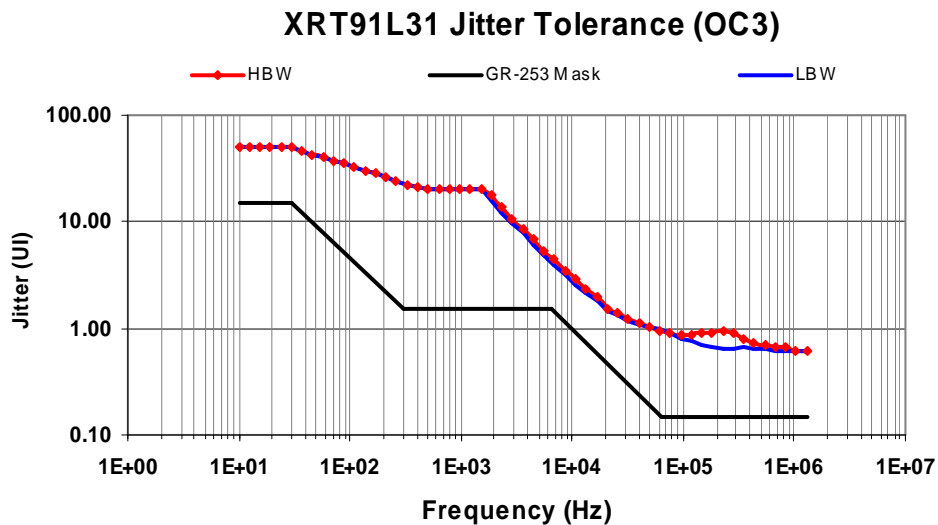


Figure 10 Jitter tolerance for OC3, 19.44 and 77.76Mhz

6.2. XRT91L31 Jitter Transfer Results

The Low bandwidth mode is selected by connecting pin 15 to Low (Gnd)

In this configuration, the CDR bandwidth is optimized to meet the jitter transfer as well as jitter tolerance specs.

6.2.1. OC12, Low Bandwidth

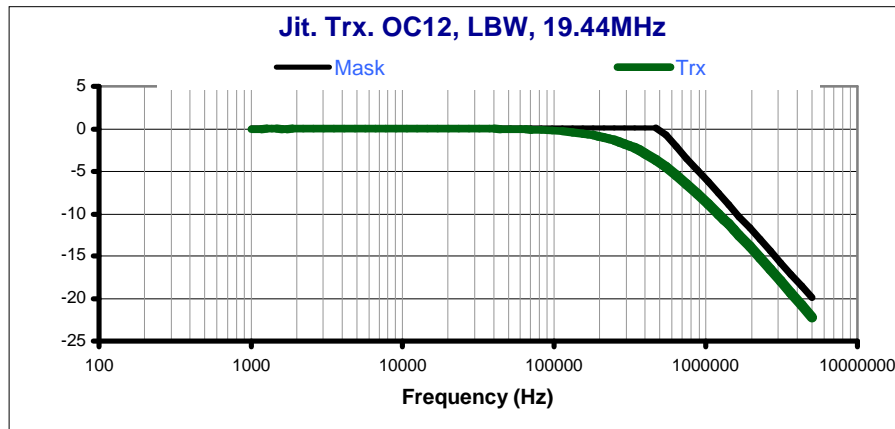


Figure 2 Jitter Transfer OC12, Low BW

6.2.2. OC3, Low Bandwidth

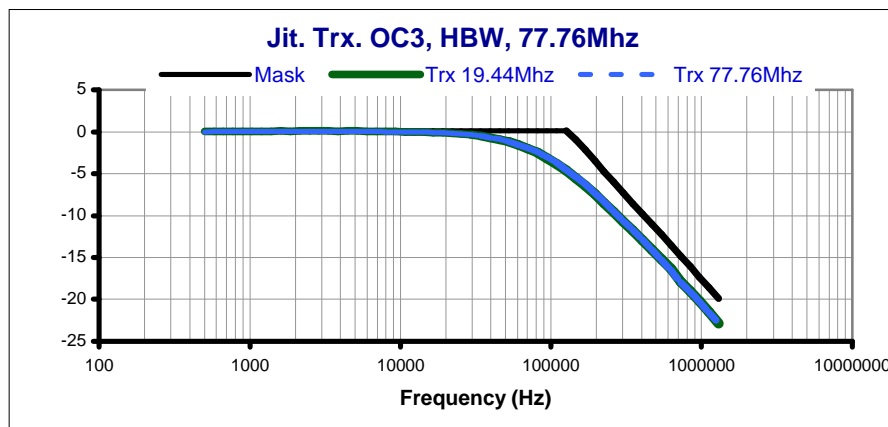


Figure 14 Jitter Transfer OC3, Low BW

6.3. OC3/OC12 Intrinsic Jitter Results:

Intrinsic Jitter Generation measurements were taken for OC12 /OC3 with an Infineon Multi-rate SFP, with 19.44MHz.

For OC12, the Omniber filter settings are 12KHz to 5 MHz.

For OC3, the Omniber filter settings are 12KHz to 1.3 MHz

	Speed	Peak to Peak (0.1 UI spec)	RMS (0.01UI spec)
XRT91L31	OC12	0.083	.005
	OC3	0.048	0.002

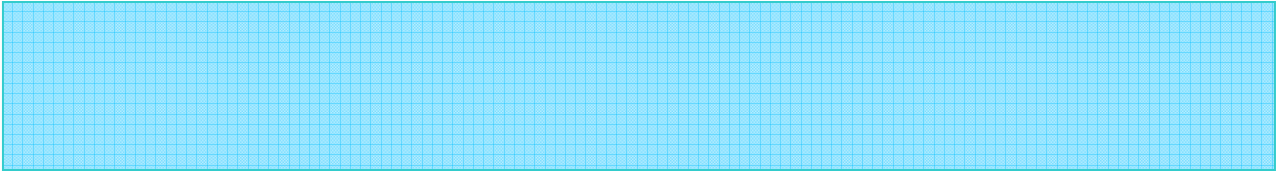
Table 1 Intrinsic Jitter Generation Performance

7. Conclusion:

Jitter tolerance, Jitter transfer and Intrinsic Jitter Generation performance of EXAR XRT91L31 is measured.

It is clearly seen that the XRT91L31 with standard optics has very good Intrinsic Jitter Generation as well as jitter Tolerance performance with a lot of margin. The XRT91L31 also passes Jitter Transfer specs (with pin 15 configured to be low).

The XRT91L31 enables the design of a single board to meet all 3 jitter specifications, or it can work in pin compatible mode with the VSC 8117 and get comparable performance. The XRT91L31 has a further benefit of being a CMOS device and consumes less power.



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